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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,016	09/30/2003	Satoru Miyagi	100021-00133	2380

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,016	MIYAGI, SATORU	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/30/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 3-8, 14, 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, as well as other claims, "slowly" is indefinite because it is a relative term that has not been defined in the specification or claims. Thus, it cannot be determined how slowly (or quickly) the control signal must transition in order to be within the scope of claim 3. Thus, this term should be removed from claim 3, and all other claims in which it appears.

The same problem exists for the terms "large" and "small" in claim 5.

In claim 7, "normal" is an improper term that should also be removed from the claims (because this term has not been clearly defined in the specification or claims).

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 8, 9, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Mashiko.

As to claims 1 and 8, note Figs. 1 and 12(A) of Mashiko, where the recited "high-threshold N-channel MISFET" reads on FET Q3 (it is a MISFET using the definition provided by applicant on the last eight lines of page 1 of the instant specification); the recited "load circuit" reads on circuit 11; the recited "psuedo high-potential power supply line" reads on VDD_V; and the recited "real low-potential power supply line" reads on GND.

As to claims 3, 4, 14 and 15, the recited "waveshaping circuit" reads on either circuit 15 or the combination of circuits 13 and 15.

As to claim 9, the recited "level conversion circuit" reads on circuit 13, and the recited first and second control signal levels are the levels of S1 and SL.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5-7, 10-13 and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashiko.

As to claims 2, 12 and 13 the recited backgate biasing, though not disclosed by Mashiko, nevertheless would have been obvious to those having ordinary skill in the art at the time of applicant's invention because it is old and well-known in the art to bias load FET as claimed (note applicant's admitted prior art Fig. 1E, for example).

As to claims 5 and 18, official notice is taken by the examiner that it is also old and well-known in the art to use high Vt FETs in pumping and MUX circuits (such as those within circuits 13 and 15 in Mashiko's Fig. 1).

As to claims 6, 7, 19 and 20, it is also old and well-known in the art that control signals (such as signal S1 in Mashiko) are digitally generated by a processor, and then converted into analog form for controlling gates of FET's (such as the pull-up FETs disclosed by Mashiko).

As to claim 10, it is also old and well-known in the art to form IC components, such as those of Mashiko, together in a module.

As to claim 11, those having ordinary skill in the art will easily recognize that the first level in Mashiko (i.e., the level of signal S1) is a relatively low level (because it needs

to be boosted), which should be made equal to interface potentials within load circuit 11 (also relatively low levels).

As to claims 16 and 17, the recited signal wiring shield and layering arrangement does not define patentably over Mashiko because these are also old and well-known structures in the art of semiconductor technology, official notice again being taken by the examiner.

Claims 21 and 22 only differ from Mashiko's circuitry in reciting that the psuedo and/or real power supply lines are "brought outside a chip". Though not disclosed by Mashiko, such would have been obvious because those having ordinary skill in the art know that on a printed circuit board, there are many load circuits (such as load circuit 11 in Mashiko) formed thereon, and separate IC's are supplied with a common power supply signal (thus requiring that the supply lines be "brought outside" the IC's.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note NFET 30 in Fig. 3 of Kurotsu, NFET 41 in Fig. 5 of Nakano, NFET Q15 in Fig. 3 of Son et al, and NFET 403D in Fig. 4D of Burr.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth Wells/
Kenneth B. Wells
Primary Examiner
Art Unit 2816

July 9, 2004